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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHUNG, PHUNG M	

ART UNIT	PAPER NUMBER
2117	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/668,651	ADAMS ET AL.	
	Examiner	Art Unit	
	Phung My Chung	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/27/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Hughes (6,373,758).

As per claims 1-4, Hughes et al disclose a method for repairing defective memory elements using self-test circuitry in a memory having a plurality of memory elements including a first memory element and a second memory element (Fig. 5), comprising:

Counting fails in the first memory element with a counter (507);

Counting fails in the second memory element with the counter (507);

Comparing the number of fails in the first memory element to the number of fails in the second memory element;

Determining the one of the first memory element and the second memory element having the most fails; and

Allocating a redundant memory element to replace the one of the first memory element and the second memory element having the most fails. (See Fig. 5, col. 10, lines 49-67 to col. 11, lines 1-39).

As per claim 5, Hughes further discloses wherein the memory is identified as unrepairable when the number of memory elements having fails exceeds the number of redundant memory elements. (See col. 10, lines 41-42).

As per claim 6, Hughes further discloses wherein the redundant memory element replaces the first column or the second column only if one or more fails are counted in the first column or the second column (Fig. 5, col. 10, lines 49-67 to col. 11, lines 1-39).

As per claim 7, Hughes further discloses wherein the plurality of memory elements include a plurality of columns and the redundant memory element includes a redundant column (Fig. 5, col. 10, lines 49-67 to col. 11, lines 1-39).

As per claim 8, Hughes further discloses wherein the plurality of memory elements include a plurality of rows and the redundant memory element includes a redundant row (Fig. 5, col. 10, lines 49-67 to col. 11, lines 1-39).

As per claim 9, Hughes further discloses wherein the plurality of memory elements includes a plurality of input/outputs and the redundant memory element includes a redundant input/output (Fig. 5, col. 10, lines 49-67 to col. 11, lines 1-39).

As per claim 10, Hughes further disclose wherein the memory further comprises a second plurality of redundant memory elements perpendicular to the plurality of redundant memory elements, the method comprising designating one of the memory elements as a must fix memory element (saturate or exceeded the number of faults allowed) if a number of fails for that one of the memory elements exceeds a number of

the second plurality of redundant memory elements available for allocation (col. 10, lines 29-48).

As per claims 11-14, these claims are rejected under similar rationale as set forth in claim 1.

As per claim 15, these claim is rejected under similar rationale as set forth in claim 1.

As per claims 16-18, Hughes discloses an apparatus comprising: a memory having a plurality of memory elements;

a redundant memory element suitable for replacing at least one of the plurality of memory elements;

a self-test circuit that tests the memory and allocates the redundant memory element to one of the plurality of memory elements if a defect is found, the self-test circuit including a multiplexer (503) that selectively couples memory outputs to a fault counter (507) that counts fails in each one of the plurality of memory elements tested by the self-test circuit;

a compare circuit that compares the number of fails in each of the memory elements and records the memory element having the most fails. (See Fig. 5, col. 10, lines 49-67 to col. 11, lines 1-39).

As per claim 19, Hughes further discloses a second fault counter (508) that counts fails in a second plurality of memory elements 502)perpendicular to the plurality of elements (501), the second fault counter selectively coupled to memory outputs by a multiplexer (504).

As per claim 20, reset signal provided to the fault counter after testing of each memory element is inherent in the system of Hughes.

As per claims 21-22, the self-test circuit allocates one or more redundant rows after allocating at least one of redundant columns or redundant input/outputs. (See col. 10, lines 40-44).

As per claim 23, Hughes discloses an apparatus for repairing a memory comprising self-test circuitry for testing a plurality of memory elements, the self-test circuitry including a multiplexer, fault detection circuitry, and count compare circuitry, the multiplexer selectively coupling an output from one of the plurality of memory elements to fault detection circuitry during a self-test, and the count compare circuitry comparing the number of fails in each of the memory elements and recording the memory element having the most fails. (See Fig. 5, col. 10, lines 49-67 to col. 11, lines 1-39).

As per claim 24, Hughes further discloses wherein the fault detection circuitry includes an exclusive-or logic gate (505) that compares a memory output to an expected memory output (expected data 512).

As per claim 25, Hughes further discloses wherein the fault detection circuitry includes a counter (507) for counting fails within a memory element under test.

As per claim 26, wherein the self-test circuit provides a reset signal to the counter after testing each one of the plurality of memory elements is inherent in the system of Hughes.

As per claims 27-29, Hughes further discloses wherein the fault detection circuitry includes storage for storing fail data including a location of one of the memory

elements and a number of fails detected for the one of the memory elements. (See Fig. 7, col. 12, lines 5-30).

3. Applicant's arguments with respect to claims 1-29 have been considered but are moot in view of the new ground(s) of rejection.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phung My Chung whose telephone number is 571-272-3818. The examiner can normally be reached on Monday to Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-jacques can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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